AsahiKASEI
ASAHI KASEI MICRODEVICES CORPORATION
Sensing Products Division
1-105 Kanda Jinbocho, Chiyoda-ku, Tokyo 101-8101, Japan

Mar 27, 2015

CQ-3 Series Application Note

0. Overview

This document provides board layout tips of Asahi's current sensor CQ-3 series (including CQ-330x), in order to make the system work properly. This application note is intended to be used for inverter applications.

This document consists of 4 sections.

1. Layout Guide of Primary Conductors
2. Layout Guide of Signal Paths
3. Layout Guide of Radiation Fins
4. Others

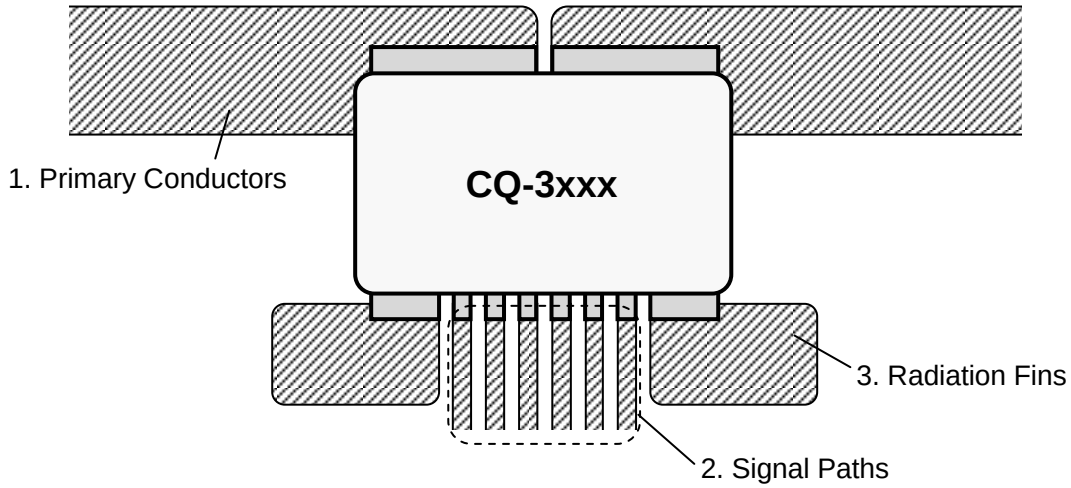
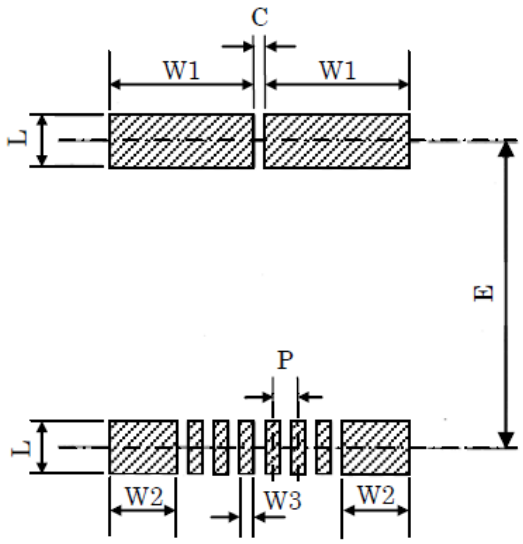


Figure 1. Layout points of CQ-3 series

1. Layout Guide of Primary Conductors

1.1. Wide and Short Traces

The traces of primary conductors should be wide and short as possible to reduce the resistance of primary conductor, which causes the heat-up of primary conductors and current sensor. It is better to make the width over 0.5mm per 1Arms when the thickness of trace layer is 0.070mm. This recommended width can be narrowed in inverse proportion to the number of trace layers used as primary conductors. It is recommended to design land pattern for conductor pins with reference to Figure 2, in order to avoid short-circuit.



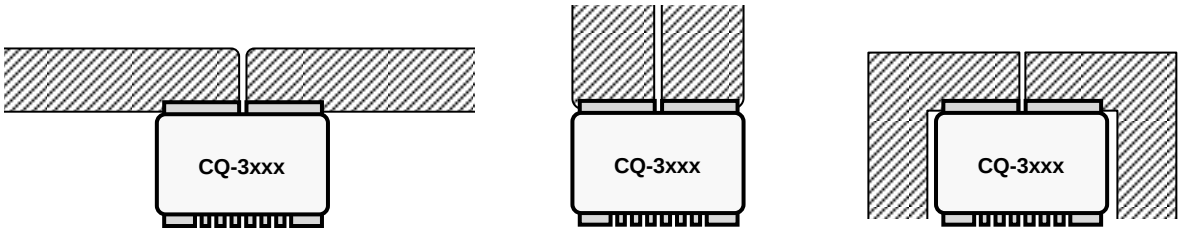
L	1.42	C	0.30
E	7.62	P	0.65
W1	3.60		
W2	1.65		
W3	0.35		

Figure 2. Recommended land pattern of CQ-3 series

Wide and short layout is also effective to reduce the stray inductance and capacitance of the primary conductors. These stray parameters cause the delay of current waveform and make the controllability of inverter systems worse.

1.2. Straight Traces

The traces of primary conductors are recommended to be drawn left to right straightly (See Figure 3a). When the traces cannot be drawn left to right because of the restriction of the board layout, the traces should be drawn toward the opposite side of signal pins (Figure 3b). Please be aware that sensitivity is slightly different by ~1% between Figure 3a and 3b. If the traces are drawn toward the signal pins, the sensitivity of the current sensor will change by ~8% at worst because of the interference of the curved traces (Figure 3c). This layout is also not recommended from a viewpoint of the interference to the signal paths.

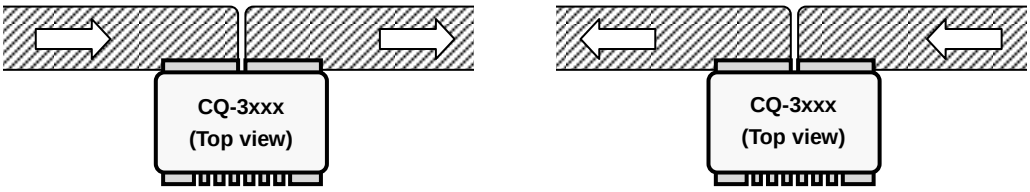


(a) Straight (recommended) (b) Curved to non-signal side (c) Curved to signal side (not recommended)

Figure 3. Current traces of CQ-3 series

1.3. Current Direction

Current direction should be considered to get the proper output. The output of CQ-3 series will normally increase when the current flows from left to right, and will decrease when the current flows from right to left (see Figure 4). If this relation is not fit to an inverter system, layouts of primary conductor should be changed to realize the opposite current direction.



(a) $V_{OUT} > V_{of}$ (b) $V_{OUT} < V_{of}$

Figure 4. The relation between sensor output and current direction in CQ-3 series

2. Layout Guide of Signal Paths

Pin names and functions of CQ-3 series are described as follows.

Table 1. Pin description

No.	Name	I/O	Description
1	TAB1	-	Radiation pin (connect to ground)
2	TEST1	-	Test pin (connect to ground)
3	VDD	PWR	Power supply pin (5V)
4	TEST2	-	Test pin (connect to VDD)
5	VSS	GND	Ground pin (0V)
6	VOUT	O	Analog output pin
7	TEST3	-	Test pin (connect to ground)
8	TAB2	-	Radiation pin (connect to ground)

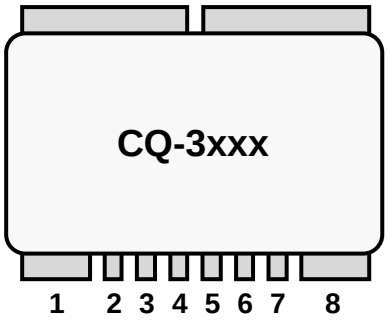


Figure 5. Pin diagram

2.1. Wide and Short Traces

The traces from VDD and VOUT pin should be wide and short as possible to reduce the interference of switching noises from the power lines.

2.2. Shielded by Ground

The traces from VDD and VOUT pin should be surrounded by the ground plane to reduce the interference of switching noises from the power lines.

2.3. Noise Filters

It is recommended to insert the 0.1μF bypass capacitor between the VDD and VSS pins to reduce the power-line noises. This bypass capacitor should be placed close by the CQ-3 series. It is better to insert another electrolytic capacitor with large capacitance to protect the CQ-3 series from an instant decrease of power supply.

In the case that there are large noises on the output, low-pass filters can be inserted to the VOUT path. This filter is recommended to be places near the MCU. Please be careful when designing the filter so as to keep the output response time required by the system.

2.4. Grounding

To avoid the unexpected operation, test pins (TEST1, TEST3) should be directly connected to ground with a short trace.

In many cases of inverter systems, the ground of MCU is separated from the main power ground to avoid the influence from the noises from switching power supply. In these cases, VSS pin of CQ-3 series should be connected to the ground of MCU, not the main power ground.

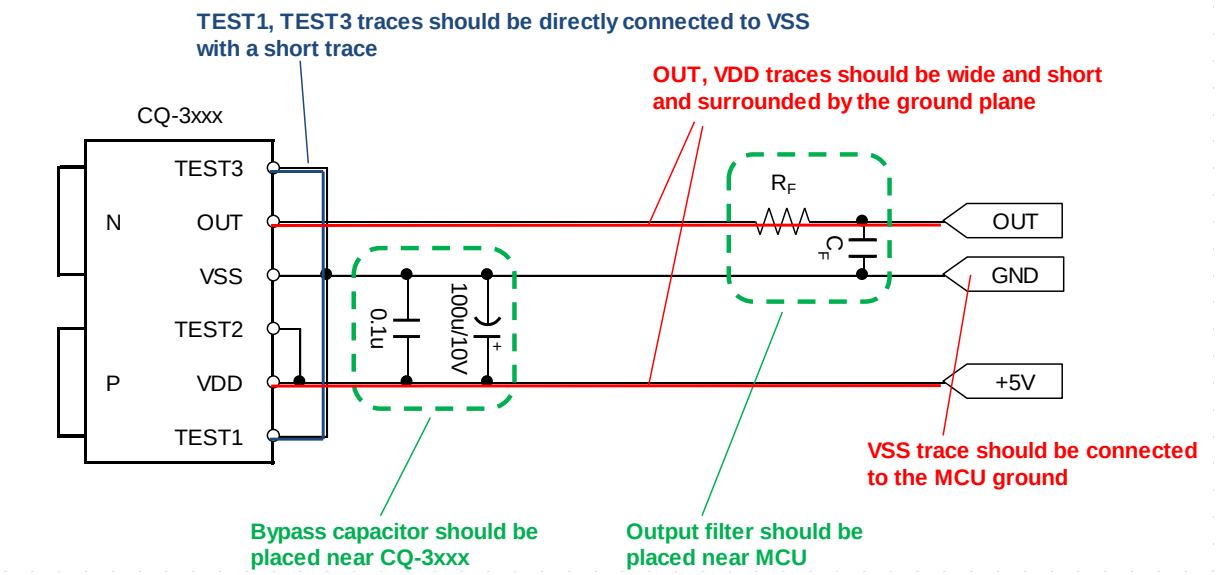


Figure 6. Circuit example of CQ-3 series

2.5. Isolation

For the assurance of working voltage of 240V, the package of CQ-3 series is designed to have >5mm creepage / clearance distance between primary conductors and signal paths, which satisfies the requirement from the safety standards of IEC/UL60950-1 (for reinforced isolation) or UL508.

If the system is required to have the isolation determined by safety standards, PCB must be also designed to have the required creepage / clearance distance between the traces for primary conductors and the traces for signal paths. This required distance will differ by the safety standards.

3. Layout Guide of Radiation Fins

CQ-3 series have two TAB pins for thermal radiation. This will reduce the temperature increase inside the package when primary current is applied through CQ-3 series. For getting better radiation performance, these two TAB pins should be directly connected to wide ground plane.

4. Others

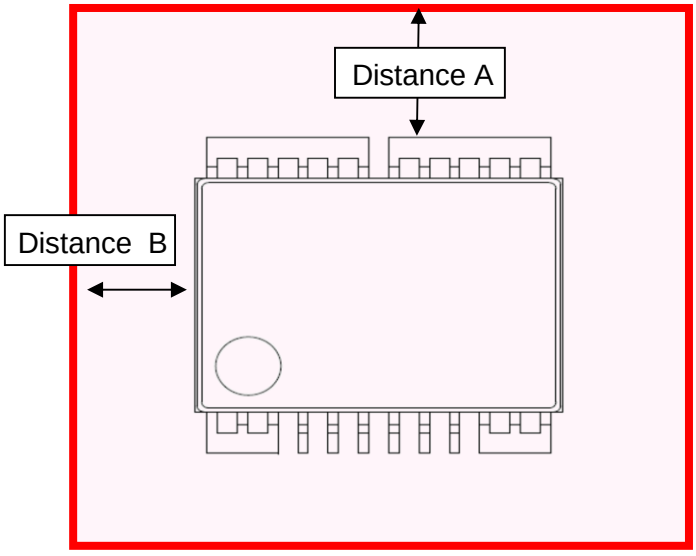
4.1. Interference from Other Current Lines

CQ-3 series are detecting magnetic flux density generated from the primary current, so are inevitably interfered from external magnetic fields. Especially in a design of board layout, care should be taken when placing other current lines around CQ-3 series. Here, other current lines mean all the current lines except the primary conductor for CQ-3 series themselves.

Basically the output error will decrease if other current lines are separated from CQ-3 series, but this relationship differs depending on the direction. Figure 7 shows the definition of direction. Distance A represents the distance toward the parallel direction of pins to pins, and distance B represents the distance toward the vertical direction of pins to pins.

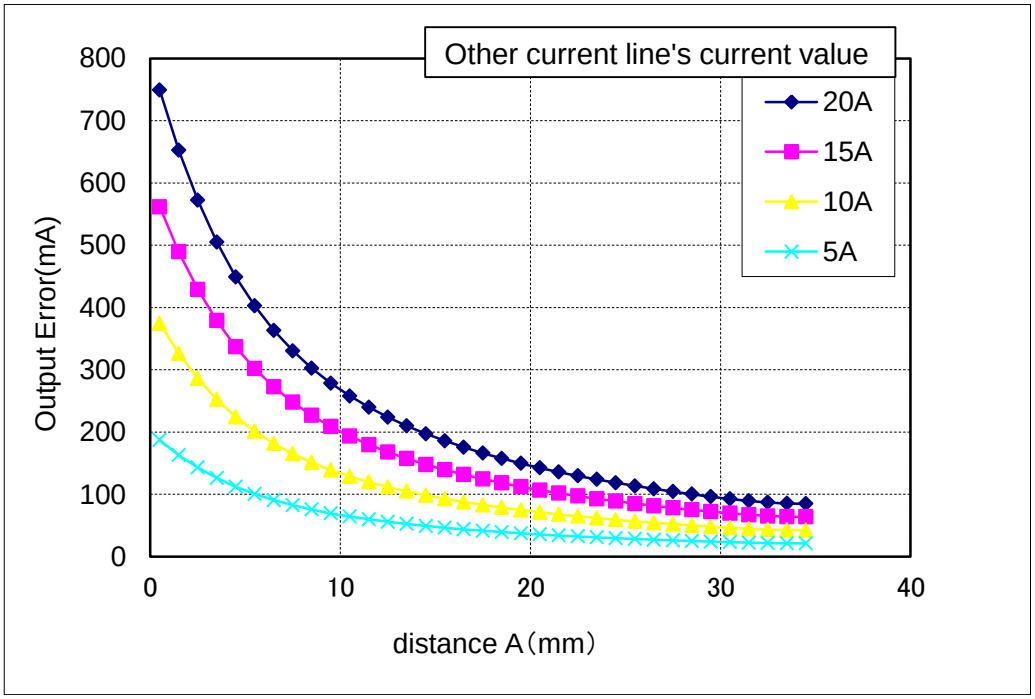
Figure 8 shows the relationship between the output error and the distance from CQ-3 series to other current lines. Legends in graphs represent the current value which flows through the other current line.

For example, to restrict the interference to 400mA (it is equal to 2% at 20A primary current) when the current value of the other current line is also 20A, distance A > 6mm and distance B > 5mm are required.

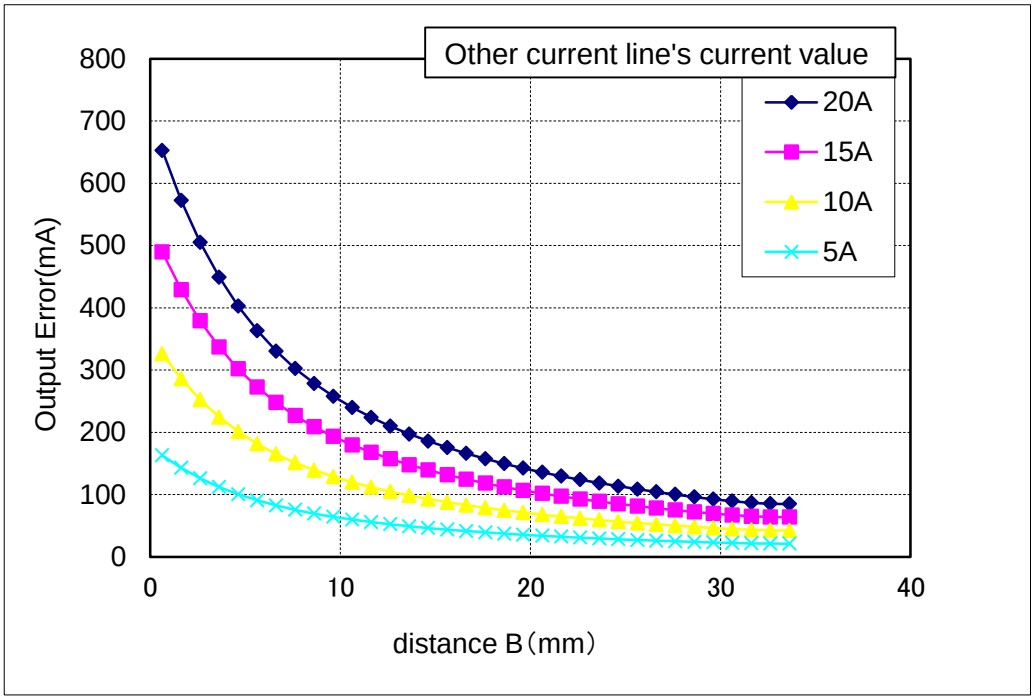


Distance A ... Distance from the edge of lead frame
Distance B ... Distance from the edge of mold

Figure 7. The definition of Distance



(a) Distance A



(b) Distance B

Figure 8. The relationship between output error and distance

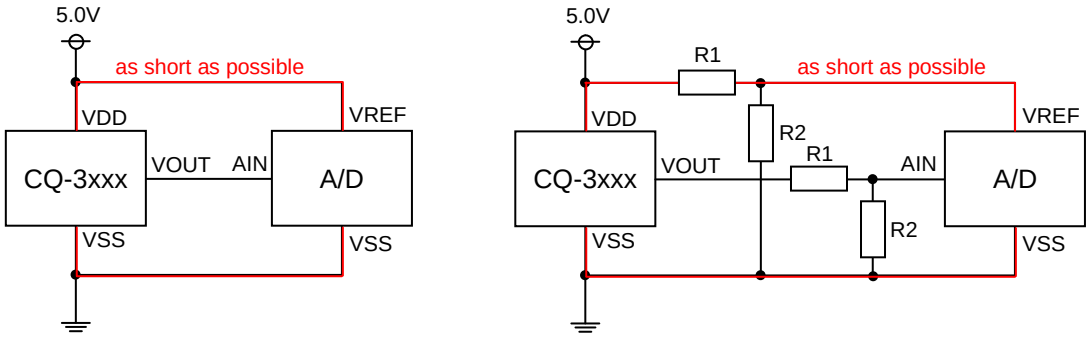
4.2. Power Supply

CQ-3 series have a ratiometric output, which is the variable output proportional to the change ratio of the supply voltage to the typical value (V_{DD}=5.0V). If the output of CQ-3 series is designed to be input to the A/D converter, this ratiometric output can be helpful to neglect the convert error caused by the reference voltage change in the A/D converter.

In the case that the reference voltage of A/D converter is 5.0V, the recommended circuit of the power supply is shown in Figure 9a. The power supply of the CQ-3 series and the reference voltage of the A/D converter should be connected directly. In this case, even if the reference voltage changes, the output voltage of CQ-3 series also changes by the same ratio as the reference voltage, which will cancel the convert error.

In the case that the reference voltage of A/D converter is below 5.0V, the reference voltage should be dropped from 5.0V supply voltage by the resistive divider (Figure 9b). For example, in the case of V_{REF}=3.3V, R1 is 4.7kΩ and R2 is 9.1kΩ. The voltage drop by a DC/DC converter or an LDO is not recommended, because these methods will cut the noise included in the 5.0V line. This will make the convert error worse.

In the both case, the board trace between the supply voltage pin of CQ-3 series and the reference voltage pin of A/D converter should be short in order to avoid the signal delay caused by the parasitic of the trace.



(a) $V_{DD}=V_{REF}$ (b) $V_{DD}>V_{REF}$

Figure 9. Recommended circuits for supply voltage

4.3. Interference from Other Magnetic Parts

CQ-3 series are also interfered by the nearby magnetic parts such as a mechanical relay and a transformer. To avoid the interference, it is recommended to avoid placing magnetic parts near the CQ-3 series and to check whether the sensitivity of CQ-3 series changes on the actual PCB.

4.4. Heat Generation

CQ-3 series must be used under the condition within the derating curve shown in Figure 10. If CQ-3 series are placed near the electric parts which produce much heat such as IPM, confirm that the ambient temperature does not exceed beyond the derating curve. (e.g. if the maximum primary current is 10A, the ambient temperature must not exceed 90°C)

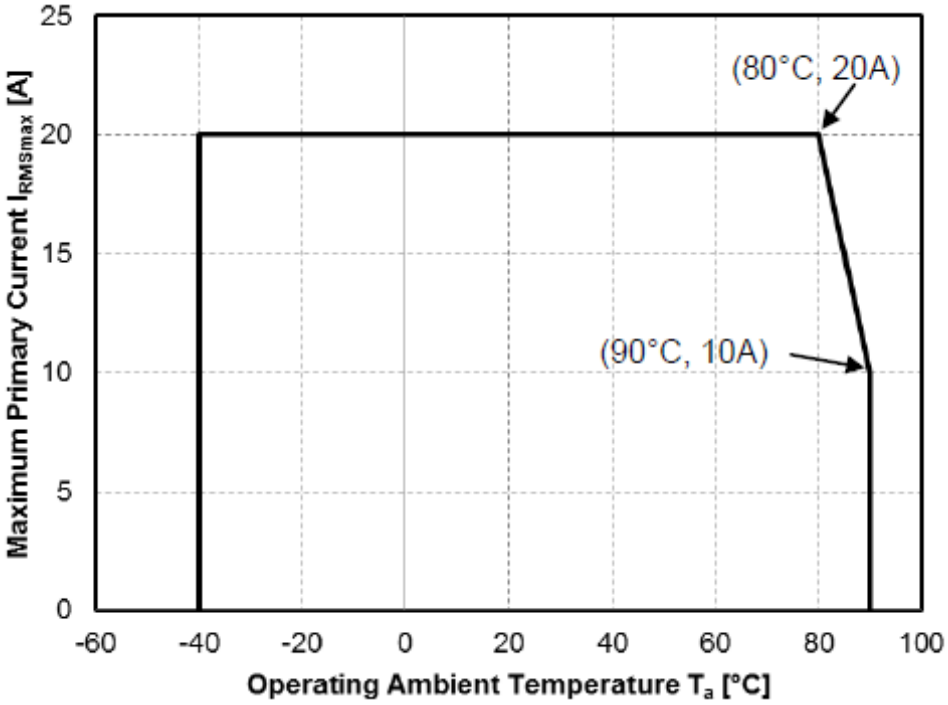


Figure 10. Derating curve of CQ-3 series

4.5. About FAQ

FAQ is on published on AKM web site.

Please access here (http://www.akm.com/akm/en/product/add/magnetic_sensors/0073/)

Disclaimer

This document is only for reference. Asahi Kasei Microdevices Corporation will not be liable for any damage and loss resulting from the use of this document.